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Comparison of a Switching Controller to two LTI Controllers for a Class of LTI Plants

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***Abstract*— We consider the design of three different control architectures for a step response tracking problem within a class of linear, time-invariant plants. Our goal is to motivate the use of a particular switching architecture that has been the subject of our prior work. We show the design of the particular switching architecture that we use and characterize its step response performance (measured in terms of the percentage overshoot and 1% settling time). We then compare the response of the switching controller to two other forms of LTI control in a servo configuration, one in which the order of the controller is unconstrained, and one in which the order of the controller is constrained to be first order (which matches the order of the dynamics of the switching controller). We shall show that, while the LTI control of unconstrained order can outperform the switching architecture, the performance improvement is bounded (in a sense to be defined). Moreover, one method of designing close-to-optimal controllers shall be discussed which yields controllers of very high order. We shall also show that the switching architecture can outperform first order LTI control and shall illustrate this via a particular design example.**

I. Introduction

The problem of stabilizing a continuous-time system via hybrid output feedback is one which has received a great amount of attention in the past decade (see, e.g., [1], [2], [4]–[12]). Our previous work has focused on a particular subproblem within this larger domain and is specifically related to stabilizability of second order linear systems via switched proportional gain feedback; [8] provides a set of necessary and sufficient conditions for which a given second order plant is stabilizable via switched proportional gain feedback, and a specific switching control law is provided when stability is possible; [9] extends the first result by considering an optimal control problem in which the objective is to stabilize a second order LTI system via switched proportional gain feedback in a manner which maximizes the rate of convergence of the state trajectory to the origin.

The goal of this paper is to apply the control laws that are obtained via the results of [8], [9] to a particular application, namely the design of switching controllers for a class of second order plants to asymptotically track step inputs. We shall attempt to assess the relative quality of these switching controllers by comparing their performance (measured in terms of overshoot and 1% settling time) to that which is achievable via two other forms of LTI control. Our first comparison shall investigate the step response performance on an LTI feedback interconnection in a *servo* configuration where the continuous-time LTI controller $K(s)$ is a rational controller of unconstrained order. Such a comparison shall allow us to obtain some information about the relative performance of our switching architecture to certain fundamental limits of LTI control in a particular feedback configuration. In the second comparison, we shall consider an LTI controller in a servo configuration with a first order controller $K(s)$. The motivation for this comparison lies in the fact that the switching architecture we consider here is a first order system. Hence, by making a comparison between a first order switching controller and a first order LTI controller, we obtain some qualitative information about the relative power of switching in our application setting.

One may naturally expect that the performance of an LTI controller of unconstrained order shall outperform a first order switching controller, and, indeed, this turns out to be the case here; however, as we shall show, the performance gap between the switching architecture and what is achievable via LTI control is *bounded* (in a sense to be defined), and an algorithm for designing LTI controllers which yield close-to-optimal performance shall be shown to produce controllers of rather high order. In the case where we restrict the LTI controller $K(s)$ to be first order, one should expect that the first order switching architecture should outperform the first order LTI controller, and we shall show that this is, in fact, the case in the context of a particular example.

The work that we present here is intended to be a condensed summary of a larger body of recently completed work. In the interest of space, no proofs or derivations are included in this document. A longer exposition which includes much more detailed explanations, along with all

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required proofs, can be found in Chapter 5 of [10].

II. Preliminaries: Plant Set, Performance Measures, and Control Constraints

In this paper, we consider a class of LTI plants of the form

$$P(s) = \frac{a}{s(s-b)} \tag{II.1}$$

where $a > 0$, $b \in \mathbb{R}$, and $b^2 < a$, i.e., second order LTI plants of relative degree two which contain a pure integrator term. Our task is the following: we shall design three different controllers (one which is a switching controller, two of which are LTI controllers) such that when the input to the controlled system $r(t)$ is a step input, i.e.

$$r(t) = \begin{cases} 0 & t < 0 \\ r & t \geq 0 \end{cases}$$

for some $r \in \mathbb{R}$, the output of the controlled plant $y(t)$ asymptotically tracks the input $r(t)$, i.e.,

$$\lim_{t\to\infty} |y(t) - r(t)| = 0.$$

In particular, we are interested in comparing the relative performance of each of the three controller designs. The measures we shall use to compare performance are the *percentage overshoot* and *1% settling time* of the corresponding zero-state step responses. For a step input of amplitude r, we define the percentage overshoot of the zero-state step response $y(t)$ as the smallest value of $M > 0$ such that

$$y(t) \leq r(M+1),$$

and we define the 1% settling time as the smallest value of $T > 0$ such that

$$|y(t) - r| \leq 0.01r \quad \forall t \geq T.$$

In all of our comparisons, we shall place a constraint on the set of admissible controllers: for a unit step input, the peak value of the control input to the plant $P(s)$, which we shall denote as $u(t)$, can never exceed 1, i.e., $|u(t)| \leq 1$ for all $t \geq 0$. The main reason for imposing such a constraint is that, without this, the 1% settling time of any of the three architectures we shall examine can be made arbitrarily small. Indeed, for each control architecture that we examine, if we allow the gain of the analog portion of the control to be unbounded, then we can achieve any 1% settling time that we desire. Imposing such a constraint implicitly imposes a restriction of the gain of the analog portion of our control and, hence, provides a "fair" basis for comparing each of our three architectures.

A brief outline of the remainder of the document is as follows: we shall first present the switching architecture that we propose for the given step-tracking problem and explain a few of the salient features of its design. We shall then characterize its step response performance for plants within the given class and shall examine the specific example in which the plant is a double integrator. Once we have completed this, we shall then present the servo architecture that we shall investigate and shall characterize the limits of LTI control in this feedback interconnection by establishing an upper bound on the ratio of the 1% settling time that is achieved by the switching architecture to the 1% settling time that can be achieved via LTI control. We shall also illustrate a method of designing LTI controllers that achieve close-to-optimal performance which, as we shall see in the context of several examples, yields very high order controllers. Finally, we shall examine the performance of a servo configuration in which the LTI control is constrained to be first order by computing the set of achievable pairs of overshoot and 1% settling time and showing that the switching controller outperforms the first order LTI controller with respect to both of these performance measures. We shall investigate this last part in the context of a specific example (again, a double integrator) but a weak generalization can be found in [10].

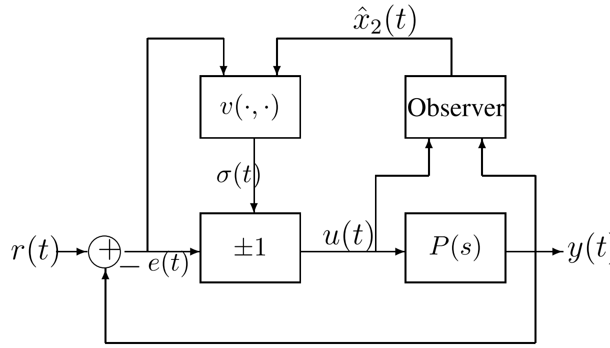


Fig. III.1. Block diagram of switching architecture to be used in designing a controller that asymptotically tracks a step input.

III. Switching Controller: Design and Performance

A block diagram of the switching architecture that we propose for the purposes of tracking a step input is depicted in Fig. III.1. Several comments are in order. First, the block labeled "± 1" switches between proportional gains of $+1$ and -1, i.e., $u(t) = e(t)$ or $u(t) = -e(t)$ for all time. It is the function of the two blocks on the upper level of the block diagram to create an appropriate switching signal $\sigma(t)$ such that the closed-loop dynamics are stable, and such that the plant output $y(t)$ asymptotically tracks the input $r(t)$ when $r(t)$ is a step. The block labeled "$v(\cdot,\cdot)$" is a memoryless switching law that takes the form

$$v(z) = \begin{cases} -1 & z'Mz \leq 0 \\ 1 & z'Mz > 0 \end{cases} \tag{III.2}$$

where $z = \begin{bmatrix} e & \hat{x}_2 \end{bmatrix}'$ and where M is a symmetric matrix. In layman's terms, the switching law $v(z)$ chooses one value of gain inside a sector of the $e - \hat{x}_2$ plane and chooses another value of the gain in a complementary sector. The block labeled "Observer" is a first order LTI system whose function is to estimate the second state of the plant $P(s)$.

Without loss of generality, one can assume that the plant has state-space description

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & \sqrt{a} \\ 0 & b \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ \sqrt{a} \end{bmatrix} u \quad \text{(III.3)}$$

$$y = x_1. \quad \text{(III.4)}$$

Informally speaking, since the output of the plant $P(s)$ is equal to the first state, the job of the first order observer is to estimate the "missing" information about the state of the plant which is encoded in the output $\hat{x}_2(t)$. The design of such an observer is a simple exercise in standard reduced-order observer design for LTI systems (see Chapter 5 of [10] for details), and the dynamics of the observer can be described in the following way:

$$\dot{x}_3 = (b - l\sqrt{a})x_3 + l(b - l\sqrt{a})y + \sqrt{a}u \quad \text{(III.5)}$$

$$\hat{x}_2 = x_3 + ly \quad \text{(III.6)}$$

where l is any real value such that $b - l\sqrt{a}$ is strictly negative (so as to ensure stable error dynamics).

While we shall not discuss this here, the memoryless switching law and first order observer were originally designed only with the objective of asymptotic stability in mind when the exogenous input $r(t) = 0$ for all time. Thus, it is fitting that one of the arguments to the memoryless switching law $v(\cdot, \cdot)$ should be the tracking error $e(t)$ since we seek to drive this error to 0 asymptotically as $t \to \infty$. Also, in addition to asymptotic stability, the control architecture of Fig. III.1 can be shown to be *finite L2 gain stable* when exogenous inputs are present, a fact we shall utilize in one of our later comparisons (see Chapters 3 and 4 of [10] for detailed explanations of both of these statements).

A. Step Response Performance of Switching Controller

Based upon the design techniques of [8], [9], we arrive at the following choice for the memoryless switching law $v(\cdot, \cdot)$:

$$v(e, \hat{x}_2) = \begin{cases} -1 & e((b - \sqrt{b^2 + 4a})e + 2\sqrt{a}\hat{x}_2) \leq 0 \\ 1 & e((b - \sqrt{b^2 + 4a})e + 2\sqrt{a}\hat{x}_2) > 0 \end{cases}. \quad \text{(III.7)}$$

Using this memoryless switching law (along with *any* observer of the form Eqn. III.5 and III.6 such that $b - l\sqrt{a} < 0$), we can prove that the zero-state step response of the output $y(t)$ has the following characteristics:

1) The step response exhibits *no overshoot*.
2) The 1% settling time of the step response T_s is given by the expression

$$T_s = \frac{1}{\delta} \ln\left(\frac{\sqrt{2}}{100}\right) + \left(1 - \frac{b}{2\delta}\right) T_1 \quad \text{(III.8)}$$

where

$$T_1 = \frac{2}{4a - b^2} \operatorname{arccot}\left(\frac{2b + \sqrt{b^2 + 4a}}{\sqrt{4a - b^2}}\right)$$

$$\delta = \frac{1}{2}\left(b - \sqrt{b^2 + 4a}\right).$$

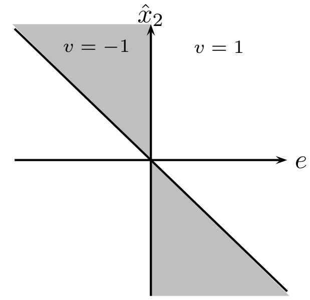


Fig. III.2. Memoryless switching law of Eqn. III.9.

We shall use the explicit characterization of T_s in the next section to compute an upper bound on the ratio of the settling time of the switching architecture to the settling time that is achievable via LTI control in a servo configuration.

B. Design Example: Double Integrator

When the plant is a pure double integrator ($P(s) = 1/s^2$), the state-space description of Eqn. III.3 and III.4 reduces to

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} u$$

$$y = x_1.$$

Plugging in values of $b = 0$ and $a = 1$ into Eqn. III.5 and III.6 and choosing a value of $l = 1$ yields the observer

$$\dot{x}_3 = -x_3 - y + u$$

$$\hat{x}_2 = x_3 + y.$$

Plugging in values of $b = 0$ and $a = 1$ into Eqn. III.7 yields the switching law

$$v(e, \hat{x}_2) = \begin{cases} 1 & e(-e + \hat{x}_2) \leq 0 \\ -1 & e(-e + \hat{x}_2) > 0 \end{cases} \quad \text{(III.9)}$$

which is depicted graphically in Fig. III.2

With the above observer and memoryless switching law in place, the zero-state unit step response $y(t)$ of the system of Fig. III.1 is shown in Fig. III.3. That the step response exhibits no overshoot is clear. The 1% settling time can be measured to be $T_s \approx 5.04$ seconds which agrees with the analytical calculation of Eqn. III.8.

IV. Comparison to LTI Control in a Servo Configuration

We now consider the servo control architecture depicted in Fig. IV.4. Here, the controller $K(s)$ is a finite order LTI controller for which the feedback interconnection of Fig. IV.4 is stable. To be consistent with our constraints in the previous section, we shall consider only those $K(s)$ for which the zero-state unit step response of the control signal $u(t)$ satisfies the constraint $|u(t)| \leq 1$ for all $t \geq 0$.

In this section, we wish to compare the settling time that can be achieved via a servo configuration to the settling time that is achieved via the switching algorithm presented in the last section. As was alluded in the introduction, it

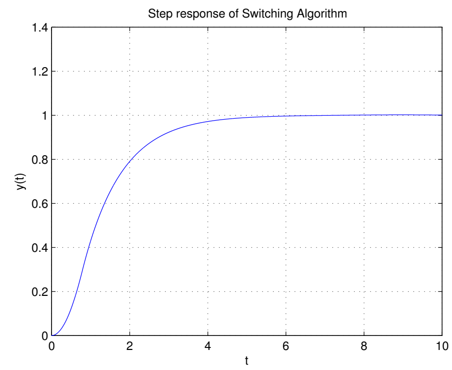


Fig. III.3. Step response of double integrator for switching architecture of Fig. III.1.

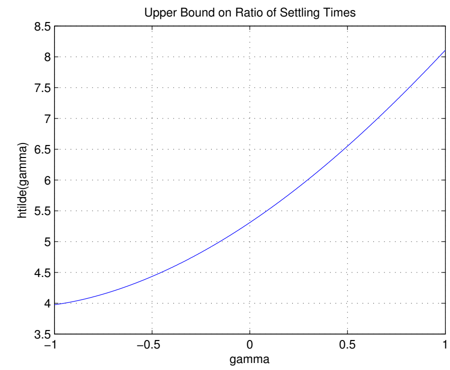


Fig. IV.5. Plot of T_s/T_l^r for $\gamma \in [-1, 1]$.

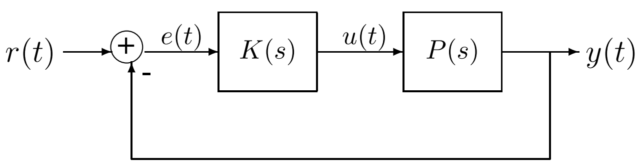


Fig. IV.4. Servo configuration.

does turn out that the servo configuration of Fig. IV.4 can achieve a smaller settling time than the settling time of the switching architecture, but as we shall discuss here, the ratio of the 1% settling time achievable via the servo configuration of Fig. IV.4 to the 1% settling time of the switching architecture is *bounded*. We shall discuss two bounds here: one which is an exact (but conservative) bound, and one which is an approximate bound. After we present each of these two bounds, we shall briefly present a method for computing controllers $K(s)$ which achieve close-to-optimal performance and shall provide results for several examples.

A. Bounds on Ratio of 1% Settling Times

We first consider the following problem: for a given plant $P(s)$ of Eqn. II.1, we wish to determine a lower bound on the time 1% settling time T_l, i.e., the smallest value of $T_l > 0$ such that, when the input $r(t)$ in Fig. IV.4 is a unit step, the output $y(t)$ satisfies

$$|y(t) - 1| \leq 0.01 \qquad \forall t \geq T_l.$$

In addition to the constraint that the step response of the control signal $u(t)$ be bounded, we also shall require that the percentage overshoot of the output step response not exceed 1%.

Once we derive a lower bound on the achievable settling time T_l, we immediately have an upper bound on the ratio of the settling time T_s/T_l. As it turns out, even though the plant $P(s)$ of Eqn. II.1 contains two free parameters, we can derive lower bounds on the 1% settling time T_l which are a function of a single scalar parameter $\gamma = b/\sqrt{a}$. The set of all $a > 0$ and b such that $b^2 < a$ is then equivalent to the set of γ that lies in the set $[-1, 1]$.

We first compute an exact lower bound on the 1% settling time T_l by computing a lower bound on the 1% *rise time* T_l^r, i.e., the smallest value of $T_l^r > 0$ such that $y(T_l^r) = 0.99$. It is clear that the 1% rise time is a lower bound for the 1% settling time T_l, and, hence, T_s/T_l^r upper bounds T_s/T_l. A set of calculations shows that, in terms of the parameter γ, we have the following exact upper bound:

$$\frac{T_s}{T_l^r}(\gamma) \leq \frac{\gamma + \sqrt{\gamma^2 + 4}}{1.9} h(\gamma)$$

where $h(\gamma)$ is given by

$$h(\gamma) = \ln\left(\frac{100}{\sqrt{2}}\right) + \sqrt{\frac{4+\gamma^2}{4-\gamma^2}} \operatorname{arccot}\left(\frac{2\gamma + \sqrt{\gamma^2+4}}{\sqrt{4-\gamma^2}}\right).$$

A plot of this upper bound for $\gamma \in [-1, 1]$ is shown in Fig. IV.5. From this plot, we determine that, over all $a > 0$, $b \in \mathbb{R}$ with $b^2 < a$, the settling time of the switching architecture is never a factor of more than roughly 8 times the settling time that can be achieved via the servo architecture. Because this bound is based upon the rise time, it tends to be rather conservative. If one makes a more concerted effort to characterize the 1% settling time more accurately, an *approximate* bound can be developed which is less conservative and is depicted graphically in Fig. IV.6. The details of how the bound is developed and why it is approximate rather than exact is too detailed to describe here, but numerical verification via several examples shows that the bound of Fig. IV.6 is typically accurate to within less than 10%.

B. Computing close-to-optimal Controllers

The approximate bound developed in the previous section indicates that an LTI controller cannot decrease the 1% settling time by roughly more than half an order of magnitude. One natural question to ask then is how can we *find* a controller which achieves close-to-optimal performance? That is, for a given $P(s)$ of the form Eqn. II.1, how can we find a corresponding controller $K(s)$ which satisfies the

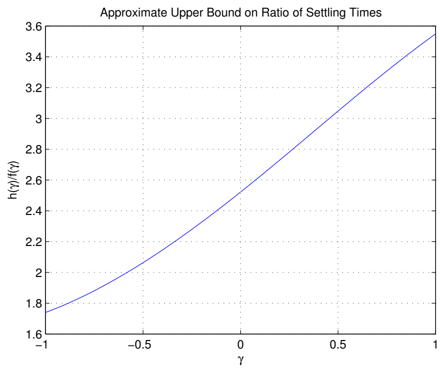


Fig. IV.6. Plot of approximate upper bound on T_s/T_l for $\gamma \in [-1, 1]$.

$P(s)$	$\hat{T}_l$	T_l	$K(s)$ Order	Switching Controller T_s
$\frac{1}{s^2}$	2	1.85	17	5.08
$\frac{100}{s(s+1)}$	0.2002	0.185	17	.4849
$\frac{1}{s(s+1)}$	2.1701	2.04	15	3.7772
$\frac{100}{s(s-1)}$	0.2002	0.193	22	.5253
$\frac{1}{s(s-1)}$	2.1701	2.08	38	7.7013

TABLE I

Summary of results for 5 different plants $P(s)$. $\hat{T}_l$ represents the *approximate* bound on the 1% settling time.

peak constraint on the control signal $u(t)$, the overshoot specification of less than 1%, and that achieves a 1% settling time that can be made arbitrarily close to the minimal possible value? To begin answering this question, it is helpful to make the following observation: suppose for the moment that we know the minimum achievable 1% settling time T_l for a given plant $P(s)$. The constraints

$$|u(t)| \leq 1 \quad \forall t \geq 0 \tag{IV.10}$$
$$y(t) \leq 1.01 \quad \forall t \geq 0 \tag{IV.11}$$
$$|y(t) - 1| \leq 0.01 \quad \forall t \geq T_l \tag{IV.12}$$

represent the boundedness constraint on the control signal (Eqn. IV.10) and the overshoot and settling time constraints on the output step response (Eqn. IV.11 and IV.12). Because these constraints are *linear* inequalities with respect to $u(t)$ and $y(t)$, they define an infinite dimensional linear program. Using a method derived by Boyd and Barrat [3] in which we parameterize $u(t)$ and $y(t)$ via the $Q-$*parameterization*, the constraints above can be relaxed into a finite dimensional linear program which can be solved numerically to find the transfer function of a stabilizing controller $K(s)$ which satisfies the peak control constraint and the overshoot constraint for a given settling time T_l. Since T_l is a parameter that must be *supplied* to the linear program, one must execute a bisection algorithm of sorts to determine the minimum achievable settling time T_l.

We present the results of using the above algorithm for five different plants in Table I. The table shows 4 quantities for each plant: the approximate 1% settling time $\hat{T}_l$ used to derive the approximate bound on the settling time ratio in the last section, the minimum 1% settling time T_l that was achieved using the linear programming formulation, the smallest order of a controller that could be found which achieves the minimal settling time, and the 1% settling time of the switching architecture we derived at the beginning of the paper (for reference). Note that the minimum 1% settling times T_l are not too far from the approximate bound $\hat{T}_l$; the largest deviation of the five plants is about 7.5%. For reference, the step response of the control signal $u(t)$ and

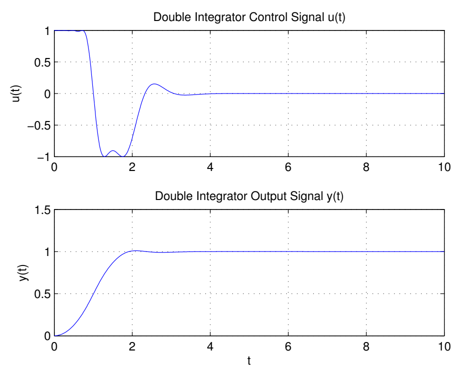


Fig. IV.7. Control signal $u(t)$ and step response $y(t)$ which yield minimal 1% settling time (1.85 seconds) for the double integrator $P(s) = 1/s^2$ using a 17th order controller.

output $y(t)$ with minimum 1% settling time are depicted for a double integrator in Fig. IV.7. It can be shown for these five examples that the ratio of T_s to T_l is within 10% of the approximate bound shown in Fig. IV.6.

Extrapolating from the examples shown here, we see that the order of the controller needed to achieve the minimal 1% settling time using this method is, generally, quite high. Using standard model reduction techniques on the controller can provide some reduction in the order of the optimal controller. For instance, using Hankel model order reduction techniques, one can reduce the optimal controller for the double integrator down from a seventeenth order controller to a twelfth order controller.

V. Comparison to First Order LTI Control in a Servo Configuration

In this section, we wish to compare the performance of the switching architecture to the performance which can be achieved via a *first* order LTI controller in a servo configuration, i.e., a controller $K(s)$ of the form

$$K(s) = k\frac{s+c}{s+d} \tag{V.13}$$

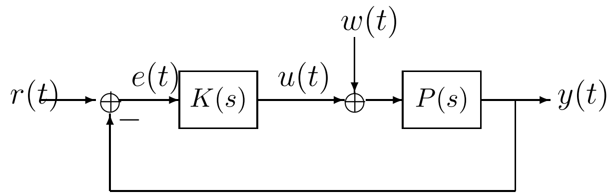


Fig. V.8. Servo architecture with plant input disturbance $w(t)$.

with $k, c, d \in \mathbb{R}$. As before, we shall impose the constraint that the step response of the control signal satisfies $|u(t)| \leq 1$ for all $t \geq 0$; however, this shall not be the only constraint that we impose on our control. Consider the servo diagram of Fig. V.8 where an exogenous input $w(t)$ has been added to the input of the plant $P(s)$. If we view the input $w(t)$ as an unwanted disturbance input, then we would like to characterize the effect of the disturbance $w(t)$ on the output $y(t)$ in some way. One way is to consider the *L2 gain* from the input $w(t)$ to the output $y(t)$, defined as the smallest value of $\gamma > 0$ such that

$$\inf_{T>0} \int_0^T (\gamma^2 w^2(t) - y^2(t))dt > -\infty.$$

The L2 gain can be viewed as a measure of sensitivity; the higher the value of the L2 gain, the more sensitive the output $y(t)$ is to the input $w(t)$.

The additional control constraint that we impose in this section is the following: for the switching system of Fig. III.1, suppose that we also introduce an exogenous input $w(t)$ to the input of the plant $P(s)$ and compute an upper bound on the L2 gain from $w(t)$ to $y(t)$ which we shall denote here as γ_s. Then, for our first order servo controller problem, we shall search *only* over those controllers $K(s)$ for which the L2 gain from $w(t)$ to $y(t)$ in the servo configuration of Fig. V.8 is no greater than γ_s. In other words, we wish to search over the set of controllers $K(s)$ which yield closed-loop sensitivity from the plant input to the plant output that are *no larger* than the sensitivity that is achieved via the switching architecture of Fig. III.1. If we do not impose such a constraint, then the "optimal" controller $K(s)$ for a given plant which achieves low 1% settling time and/or overshoot may *not* be stabilizing.

Our objective in this section is as follows: with both of the control constraints in place (the bound on the peak control value and the bound on the L2 gain), we wish to characterize the set of achievable pairs of overshoot and 1% settling time for all first order controllers $K(s)$ which satisfy each of these control constraints. We shall do this in the following manner: first, we shall compute the set of first order controllers which satisfy the two control constraints. Once we have done this, we shall numerically compute the overshoot and 1% settling time of the closed-loop step response for each of the controllers contained in this set and shall then be able to draw conclusions about performance by comparing the set of pairs of overshoot and 1% settling time that are achievable via first order servo control to the overshoot and 1% settling time that we achieve via the switching controller. We shall demonstrate this technique in the context of a specific example (again, a double integrator), but the results shown here are weakly generalizable (see [10]).

To begin, one first computes an upper bound on the closed-loop L2 gain from w to y for the switching controller of Fig. III.1 via a search over piecewise-quadratic storage functions (see Chapters 4 and 5 of [10] for details). Once this number has been computed, one begins the task of characterizing the set of controllers $K(s)$ which satisfy the two control constraints. For the double integrator example, it can be argued without loss of generality that one can choose $k = 1$ for $K(s)$ of Eqn. V.13 to satisfy the control bound constraint $|u(t)| \leq 1$ (choosing any value of $k > 1$ shall violate the constraint; choosing any value of $k < 1$ shall yield a step response with the same overshoot—but a longer 1% settling time—that can be achieved via another first order controller with $k = 1$). Now, computing the set of controllers which satisfy the L2 gain constraint amounts to determining the set of pairs (c, d) of Eqn. V.13 for which the following constraint is satisfied:

$$\left\| \frac{P(s)}{1 + P(s)K(s)} \right\|_\infty \leq \gamma_s \qquad \text{(V.14)}$$

where, here, we utilize the fact that the L2 gain from w to y for the servo configuration is equal to the H-infinity norm of the closed-loop transfer function from w to y. It can be shown in this example that the set of c and d for which the above constraint is satisfied is a compact set. We first compute an outer approximation to this set, and then finely grid the outer approximation to include only those points which satisfy the H-infinity norm constraint Eqn. V.14. Once we have completed this task, we simulate the closed-loop step responses of the resulting set of first order controllers in MATLAB and measure the overshoot and 1% settling time. The results of this process are shown in Fig. VI.9. The overshoot and 1% settling time pairs that are achievable via first order LTI control under the given peak control and L_2 gain constraints are depicted by the '$\times$' symbols, while the performance of the switching architecture that we designed in the first section is shown via the circle at the bottom of the figure for comparison. Note that the LTI control exhibits a tradeoff between percentage overshoot and 1% settling time; the minimal percentage overshoot of 26% has a settling time of 17.5 seconds, while the minimal 1% settling time of 10.5 seconds has a corresponding peak overshoot of 37%. A plot of the step response with minimal percentage overshoot and a plot of the step response with minimal 1% settling time are shown in Fig. VI.10.

Note that while we have only presented results for a single example here, the performance benefits shown here are not strictly limited to a double integrator. In [10], we examine other examples of plants $P(s)$ of the form Eqn. II.1 for which similar performance benefits exist,

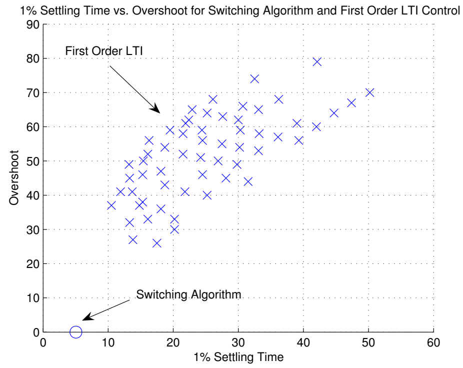


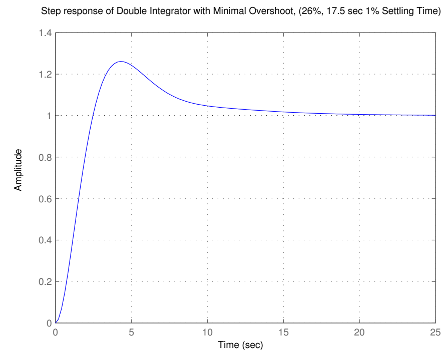
Fig. VI.9. Achievable percentage overshoot and 1% settling time time pairs that can be achieved via first order LTI control for the given peak control and L_2 gain constraints (shown by '×' in the picture). The performance of the switching architecture is shown via the circle at the bottom of the figure for comparison.

and a weak generalization is developed to extend these isolated examples into an entire class of systems for which performance benefits can be guaranteed.

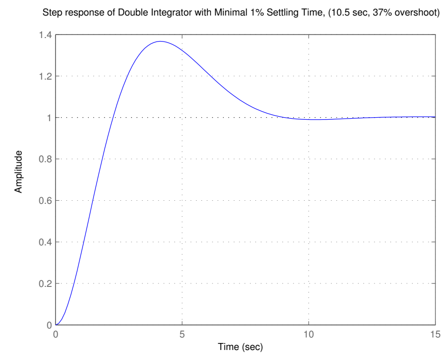
VI. Discussion

Our goal in this exposition has been to illustrate the potential utility of a particular switching controller vs. using other more traditional forms of LTI control. In comparing the performance of the switching architecture to LTI control of unconstrained order in a servo configuration, we showed that, while the servo configuration can outperform the switching architecture, it cannot outperform by typically more than half an order of magnitude. Moreover, a standard process of *finding* LTI controllers which reap these benefits yields controllers that are, in general, very high order and, hence, may be unattractive from an implementation perspective. In comparing the performance of the first order switching architecture to a first order LTI controller in a servo configuration, we showed that the introduction of switching can, indeed, increase performance.

While the work here has focused strictly on second order systems, the same techniques can be applied to classes of higher dimensional systems as well. Indeed, by invoking the Small Gain Theorem, the switching controller architecture (which was originally designed only for second order systems) can be used to design switching controllers for systems which are well-approximated by a second order LTI system in an L2 gain sense, and an example of a design for a higher order system is presented in Chapter 6 of [10].



(a) Minimal overshoot.



(b) Minimal 1% settling time.

Fig. VI.10. Step responses of double integrator that achieve minimal overshoot and minimal 1% settling time subject to the peak control value and L_2 gain bound constraints given in this section.

References

[1] Z. Artstein, Example of Stabilization with Hybrid Feedback, in *Hybrid Systems III: Verification and Control, Lecture Notes in Computer Science* 1066, Springer-Verlag, Berlin, 1996, pp. 173-185.

[2] C. Benassi and A. Gavioli, Hybrid Stabilization of Planar Linear Systems with One-dimensional Outputs. *Systems and Control Letters*, 46:303-309, 2002.

[3] S. Boyd and C. Barrat, *Linear Controller Design: Limits of Performance*. Prentice Hall, 1991.

[4] B. Hu, G. Zhai and A. N. Michel, Hybrid Output Feedback Stabilization of Two-Dimensional Linear Control Systems, *Proceedings of the 2000 American Control Conference*, pp. 2184-2188, Chicago, Illinois, June, 2000.

[5] D. Liberzon, Stabilizing a Linear System with Finite-state Hybrid Output Feedback, *Proceedings of the 7th IEEE Mediterranean Conference on Control and Automation*, 1999.

[6] E. Litsyn, Y. V. Nepomnyashchikh and A. Posonov, Stabilization of Linear Differential Systems via Hybrid Feedback Controls, *SIAM Journal of Control Optimization* Vol. 38, No. 5, pp. 1468-1480, 2000.

[7] E. Litsyn, Y. V. Nepomnyashchikh and A. Posonov, Classification of Linear Dynamical Systems in the Plane Admitting a Stabilizing Hybrid Feedback Control. *Journal of Dynamical Systems,* 6(4):477-501, 2000.

[8] K. R. Santarelli, A. Megretski and M. A. Dahleh, On the Stabilizability of Two-dimensional Linear Systems via Switched Output Feedback, *Proceedings of the 24th American Control Conference*, pp. 3778-3783, vol. 6, Portland, June 2005.

[9] K. R. Santarelli, M. A. Dahleh, and A. Megretski, Optimal Controller Synthesis for Second Order LTI Plants with Switched Output Feedback, *Proceedings of the 46th Conference on Decision and Control*, pp. 4127-4132, San Diego, December 2007.

[10] K. R. Santarelli, *On the Synthesis of Switched Output Feedback Controllers for Linear, Time-invariant Systems*, Ph. D. thesis, Massachusetts Institute of Technology, 2007.

[11] X. Xu and P. J. Antsaklis, Design of Stabilizing Control Laws for Second-order Switched Systems, *Proceedings of the 14th IFAC World Congress,* vol. C., pp. 181-186, Beijing, P.R. China, July 1999.

[12] X. Xu and P. J. Antsaklis, Stabilization of Second-order LTI Switched Systems, *ISIS Technical Report isis-99-001,* Dept. of Elec. Enging., University of Notre Dame, January, 1999.